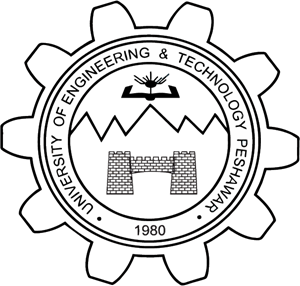
Lab Report No 6

**Decoder and Encoder**

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**Group No 5**

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**CS-202L-Digital Logic Design Lab**

**Department of Computer System Engineering**

**University of Engineering and Technology Peshawar**

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**Lab No 6: Decoder and Encoder**

**Objective:**

* To construct a decoder and an encoder and verify their truth tables

**Apparatus:**

* 3 input NAND gate (IC 7410) x2
* 2 input OR gate (IC 7432) x3
* NOT gate (IC 7404)

**Theory:**

**Decoder:**

A deecoder is a digital circuit that has multiple inputs and multiple outputs. If a decoder has ‘n’ number of input then it will have maximum ‘2n’ number of outputs. We can set any output for a specific input in binary for a decoder. Here we will make a commercial decoder whose output gives us minterms or maxterms depending on high or low as active for the corresponding input. There is also one extra input which is called enable. It switch on or switch off the decoder.

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Commercial Decoder Truth Table (3x8)

**Encoder:**

An encoder is the opposite of the decoder. It also has multiple inputs and multiple outputs but the inputs are ‘2n’-bit and the output is ‘n’-bit. As decoder we can also set any output for the encoder. Commercial encoders has minterms or maxterms as inputs and the output is corresponding binary number. These encoders can only one input out of 2n inputs as ‘1’ or ‘0’ depending on low as active or high as active. If there is more than one 1’s then it will show some random output which will not be correct.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| D0 | D1 | D2 | D3 | A | B |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 |

Commercial Encoder Truth Table (4x3)

**Verification of Decoder and Encoder**

**Decoder 2x4:**

Here we will create 2x4 decoder with an enable input. This decoder will have low as active.

**Circuit:**

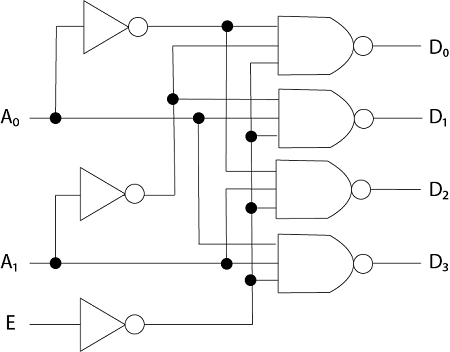


Fig 01: 2x4 Decoder Circuit

**D0 = (A0’ A1’ E’)’**

**D1 = (A0’ A1 E’)’**

**D2 = (A0 A1’ E’)’**

**D3 = (A0 A1 E’)’**

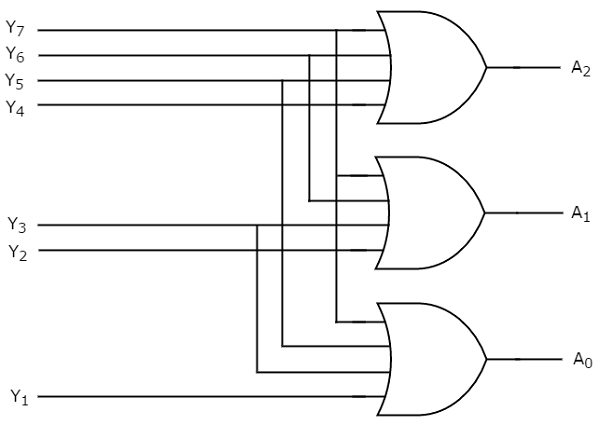
**Truth Table:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| A0 | A1 | E | D0 | D1 | D2 | D3 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 |

Truth table for verification

**Encoder 8x3:**

This encoder will have inputs and three outputs.

**Circuit:**

A0 = Y4 + Y5 + Y6 + Y7

A1 = Y2 + Y3 + Y6 + Y7

A2  = Y1 + Y3 + Y5 + Y7

**Truth Table:**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 | A0 | A1 | A2 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

Truth table for verification